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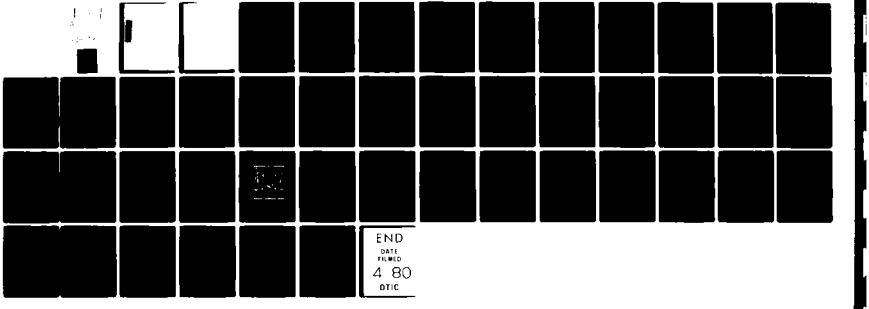

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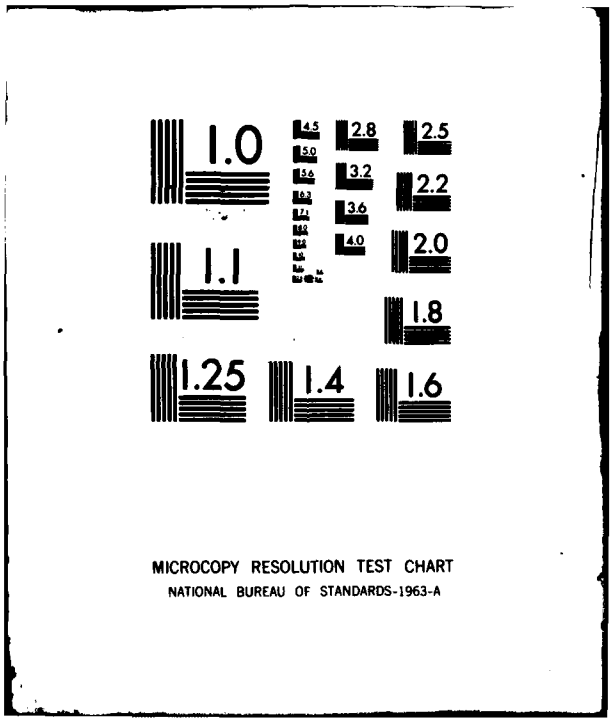

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LINCOLN LABORATORY

TRANSCONDUCTANCE MULTIPLIERS FOR WEIGHT CIRCUITS IN AN ADAPTIVE NULLING SYSTEM

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Group 68

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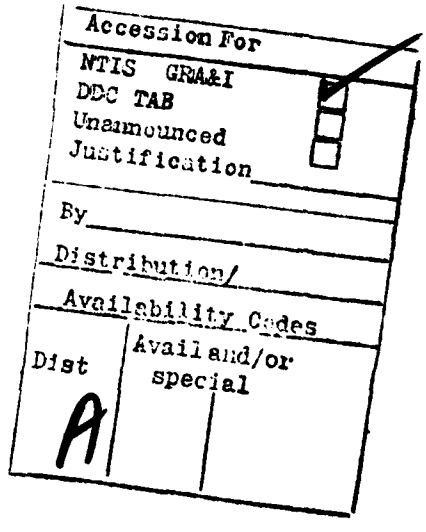
ABSTRACT

The design, construction, and measurement of weight circuits utilizing four-quadrant transconductance multiplication is described. The weights operate over a 10 MHz band centered at 121.4 MHz.



CONTENTS

I. INTRODUCTION

The problem of adaptive filtering requires a generalized filter topology with electrically adjustable parameters. Such a topology is shown in Fig. 1. The inputs $x_i(t)$ (i=1, ..., N) are different versions (for example, time delayed versions) of the same signal, and filtering is obtained by summing these inputs in an appropriately weighted manner. The weight given each input $x_i(t)$ is controlled by a weight setting, w_i.

The application for the weight circuits to be described in this Note was an adaptive antenna system [Ref. 1], in which the inputs were the IF signals from various antenna ports. In such a system, it is of importance that the weight circuits provide complex weighting (that is, that they provide both amplitude and phase adjustment to the input signals). The topology used for these weight circuits is shown in Fig. 2. The input is split into in-phase and quadrature components with a 90° hybrid power splitter. Each component is independently multiplied by a (real) weighting factor, and then the two are recombined using a 0° hybrid power combiner. The resulting weight setting, in complex form, is $V_I - jV_Q$.

The general design goals for these weight circuits were as follows.

1. Signal path bandwidth of 116.4 MHz - 126.4 MHz, minimum.
2. Control path bandwidth of DC - 0.5 MHz, minimum.
3. A high degree of linearity in the signal path (i.e., to keep the third order intermodulation products low for signal levels below the 1.0 dB compression point).
4. At least a moderate degree of linearity in the control path (i.e., to keep the gain vs. control voltage characteristics of the in-phase and quadrature multipliers nearly linear).
5. Input and output VSWR less than 1.2.
6. Accurate channel-to-channel tracking between weights (i.e., to keep the slopes of the amplitude and phase responses of the weights as nearly equal as possible).

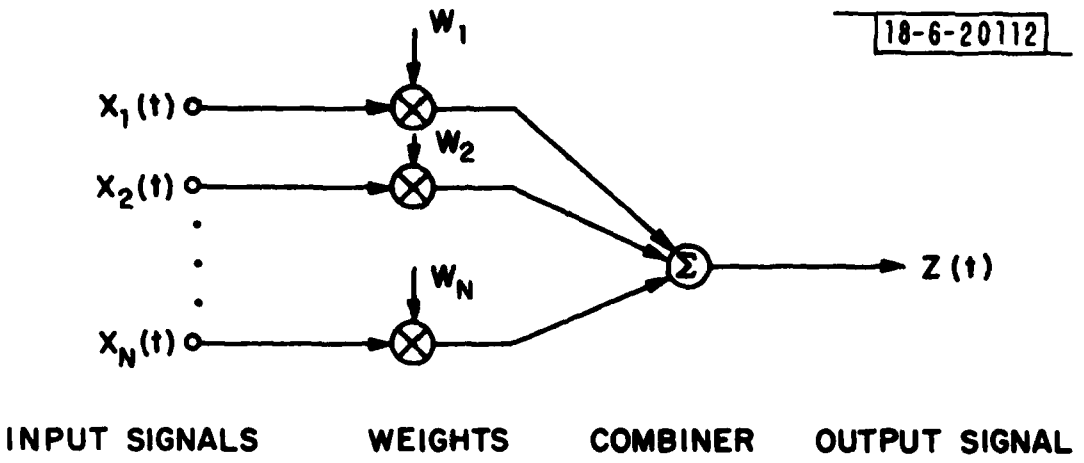


Fig. 1. Adaptive filter topology.

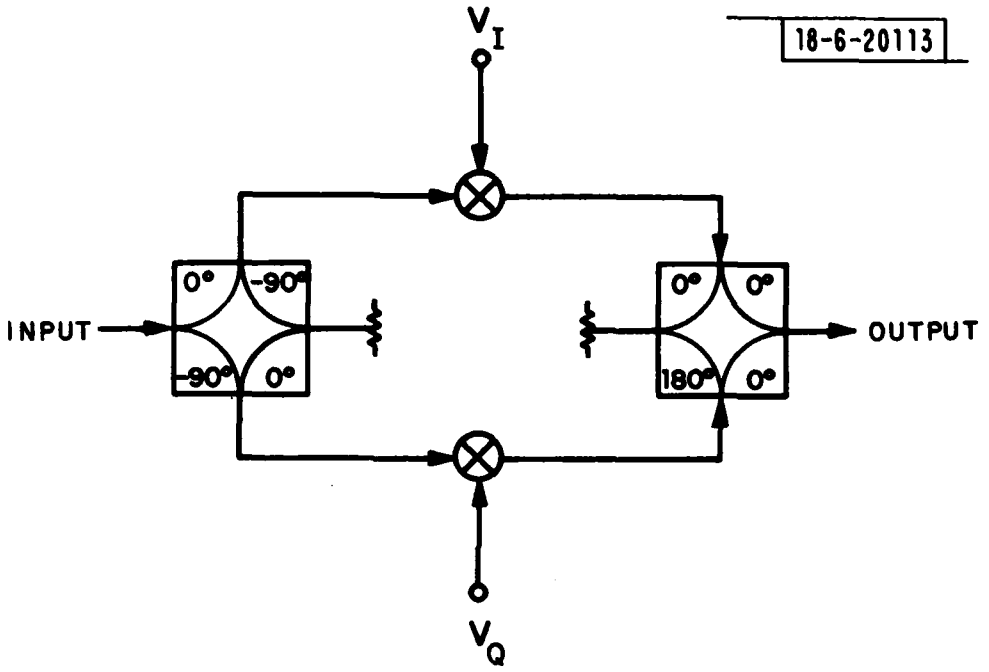


Fig. 2. Weight circuit topology.

7. The effective elimination of weight feedthrough as a source of error.

The presence of frequency-dependent feedthrough in weight circuits can severely limit achievable depth-of-null performance in a wideband nulling system. Because of this, the last goal mentioned above was considered a prime one.

Four-quadrant transconductance multipliers have several inherent virtues that make them appealing for use as weight circuits in adaptive nulling systems. They are inherently wide band for any attenuation setting. The physical principle of four-quadrant transconductance multiplication is inherently linear. Input and output impedance characteristics can be well controlled. They have no obvious inherent feedthrough mechanism. However, it appears that all the published work in this area focuses on DC characterization of the technique to the virtual exclusion of potential dynamic limitations. This Note addresses some of the issues involved in the successful implementation of eight weights, operating over a 10 MHz bandwidth centered at 121.4 MHz, using transconductance multiplication.

II. FOUR-QUADRANT TRANSCONDUCTANCE MULTIPLICATION

Four-quadrant transconductance multiplication, as originally described by Gilbert [Ref. 2], consists essentially of six matched, isothermal, ideal transistors with infinite current gain in one of two topologies. The so-called inverted form, shown in Fig. 3, is the one chosen for this application and discussion will be limited to this topology.

If all collector currents are assumed to be much larger than the saturation current, I_s, of the transistors, such that, by the ideal diode equation,

$$i_c = I_s\left\{\exp\left(\frac{qv_{BE}}{kT}\right) - 1\right\} \simeq I_s \exp\left(\frac{qv_{BE}}{kT}\right) \qquad (1)$$

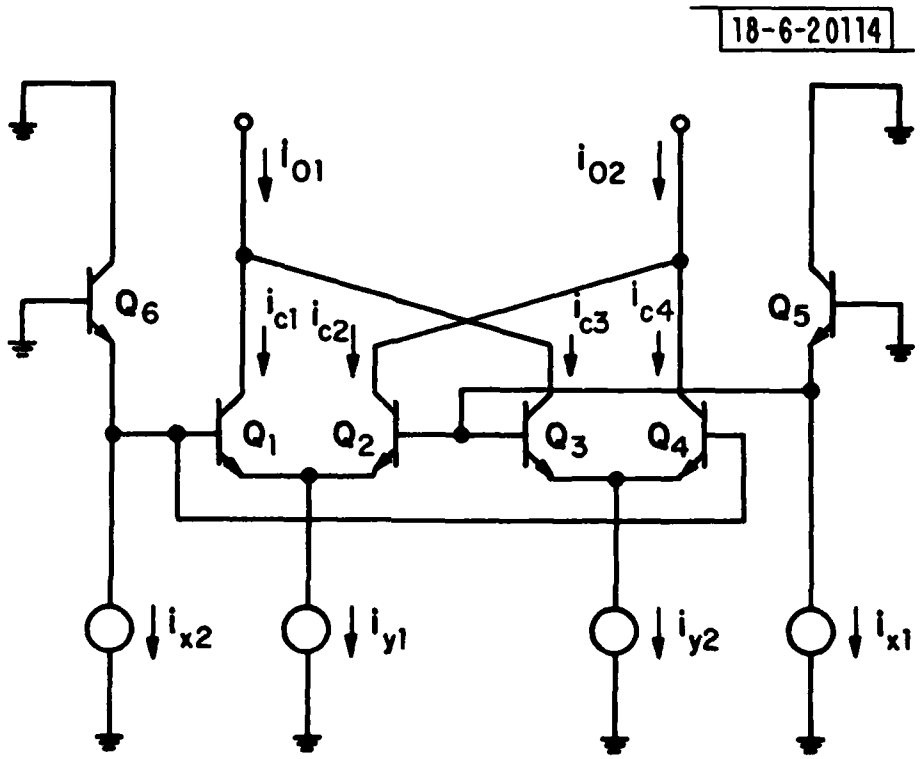


Fig. 3. Transconductance cell.

where

q = electron charge

k = Boltzmann's constant

T = temperature

Then, going around the $Q_6Q_1Q_2Q_5$ loop,

$$-\frac{kT}{q}\log\frac{i_{x2}}{I_s}-\frac{kT}{q}\log\frac{i_{c1}}{I_s}+\frac{kT}{q}\log\frac{i_{c2}}{I_s}$$

$$+\frac{kT}{q}\log\frac{i_{x1}}{I_s}=0 \qquad (2)$$

yielding

$$\frac{i_{c1}}{i_{c2}}=\frac{i_{x1}}{i_{x2}} \quad . \qquad (3)$$

Using the identity,

$$i_{c1}+i_{c2}=i_{y1} \qquad (4)$$

and substituting in (3) yields

$$i_{c1}=\frac{i_{x1}}{i_{x1}+i_{x2}}\,i_{y1}$$

$$i_{c2}=\frac{i_{x2}}{i_{x1}+i_{x2}}\,i_{y1} \quad . \qquad (5)$$

Similarly for the $Q_5Q_3Q_4Q_6$ loop,

$$i_{c3}=\frac{i_{x2}}{i_{x1}+i_{x2}}\,i_{y2}$$

$$i_{c4}=\frac{i_{x1}}{i_{x1}+i_{x2}}\,i_{y2} \quad . \qquad (6)$$

Thus,

$$i_{o1} = \frac{i_{x1}i_{y1}+i_{x2}i_{y2}}{i_{x1}+i_{x2}}$$

$$i_{o2} = \frac{i_{x2}i_{y1}+i_{x1}i_{y2}}{i_{x1}+i_{x2}} \quad . \tag{7}$$

If purely differential inputs are assumed, such that

$$i_{x1} = \frac{(1+x_d)}{2} I_x \qquad -1 \leq x_d \leq +1$$

$$i_{x2} = \frac{(1-x_d)}{2} I_x$$

$$i_{y1} = \frac{(1+y_d)}{2} I_y \qquad -1 \leq y_d \leq +1$$

$$i_{y2} = \frac{(1-y_d)}{2} I_y \tag{8}$$

then the two outputs are

$$i_{o1} = \frac{(1+x_d y_d)\ I_y}{2}$$

$$i_{o2} = \frac{(1-x_d y_d)\ I_y}{2} \quad . \tag{9}$$

If the output is taken differentially such that

$$i_{od} = i_{01} - i_{02} \tag{10}$$

then

$$i_{od} = x_d y_d I_y \tag{11}$$

which illustrates the multiplicative property of this topology. Note that, ideally, either i_{o1} or i_{o2}, appropriately AC coupled, could be used as the output.

In a more graphic sense, one can picture the Q_1Q_2 and Q_3Q_4 differential pairs as current dividers, controlled and linearized by the Q_5Q_6 pair. By appropriately steering the incremental currents $\frac{y_d}{2} I_y$ and $-\frac{y_d}{2} I_y$, the collector currents can be summed and differenced to provide an output over the range $-y_d I_y$ to $+y_d I_y$. This is illustrated in Figs. 4a and 4b. Here, the incremental currents at various points in the circuit of Fig. 3 are represented vectorially. Two cases are shown, one with $x_d = \frac{1}{2}$ and one with $x_d = 0$.

In practice, the incremental input currents are usually provided by straightforward voltage-to-differential current stages, such that

$$x_d = \frac{g_x v_x}{I_x} \tag{12}$$

$$y_d = \frac{g_y v_y}{I_y} \tag{13}$$

and the output voltage is obtained with load resistors, so the final transfer function is of the form

$$v_o = v_x v_y \left(\frac{g_x g_y R}{I_x}\right) \tag{14}$$

where v_x and v_y are the respective input voltages and g_x and g_y are the respective transconductances of the x and y input stages and R is the output load resistance.

It should be noted that all the transistors in the transconductance cell are operated in common base or emitter coupled configurations. Very wide-band performance can thus be achieved, limited essentially by the f_T's* of the transistors employed. Furthermore, this bandwidth is relatively independent of the input signals.

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*The f_T of a transistor is that frequency at which the current gain of the device has fallen to unity. The transistor types chosen for this application have f_T's specified at slightly over 1 GHz.

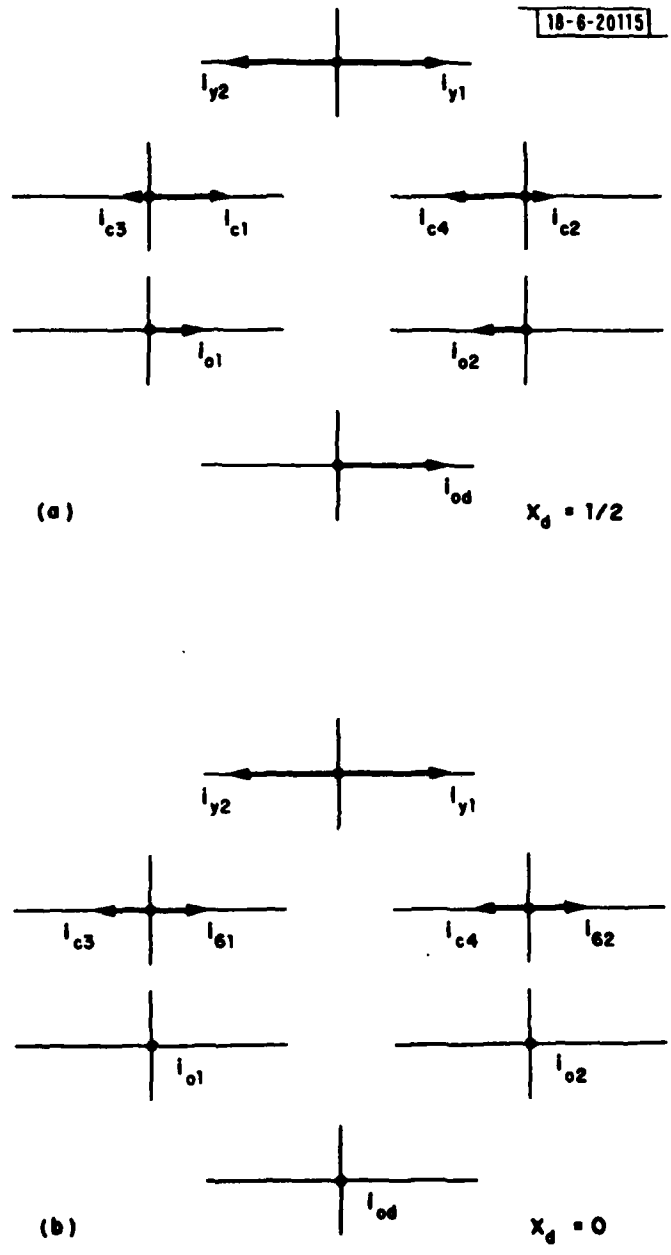

Fig. 4. Vectorial representation of ideal transconductance cell incremental currents for two values of x_d. (Differential inputs assumed.)

III. DC ERRORS

The DC response of a transconductance cell operated in a differential fashion may be viewed as a surface (i.e., a hyperbolic paraboloid) described ideally by Eq. 11, lying above the $x_d y_d$ plane. In fact, the surface will be distorted due to the non-ideal response of any real circuit. If the distortion is small and sufficiently smooth, then the response can be approximated by the two dimensional power series

$$i_{od} \tilde{=} (a_0 + a_1 x_d + a_2 y_d + a_3 x_d^2 + a_4 x_d y_d + a_5 y_d^2 + a_6 x_d^3 + \ldots + a_{14} y_d^4)\, I_y \tag{15}$$

which experience shows can be approximated* by

$$i_{od} \tilde{=} [(b_3 x_d^3 + b_2 x_d^2 + b_1 x_d + b_0)(c_3 y_d^3 + c_2 y_d^2 + c_1 y_d + c_0) + (d_0 + d_1 x_d + d_2 y_d + d_3 x_d^2 + d_4 y_d^2 + d_5 x_d^3 + d_6 y_d^3 + d_7 x_d^4 + d_8 y_d^4)]\, I_y \tag{16}$$

The form of Eq. 16 can be used to develop the model shown in Fig. 5. The effects are twofold:

1. Non-linearities are introduced into the desired signal paths.
2. New signal paths (i.e., feedthrough paths) are introduced and they are, in general, non-linear.

The terms of Eq. 16 can then be identified in modeling terms as:

$b_0(c_0)$ – equivalent offset in the x(y) signal path

---

*The accuracy of Eq. 16 in describing transconductance multipliers depends in large measure on the distortion being small and the cross product of higher order terms (e.g., $x_d^2 y_d^2$) being negligible. The fact that this condition holds is analytically and experimentally demonstrable.

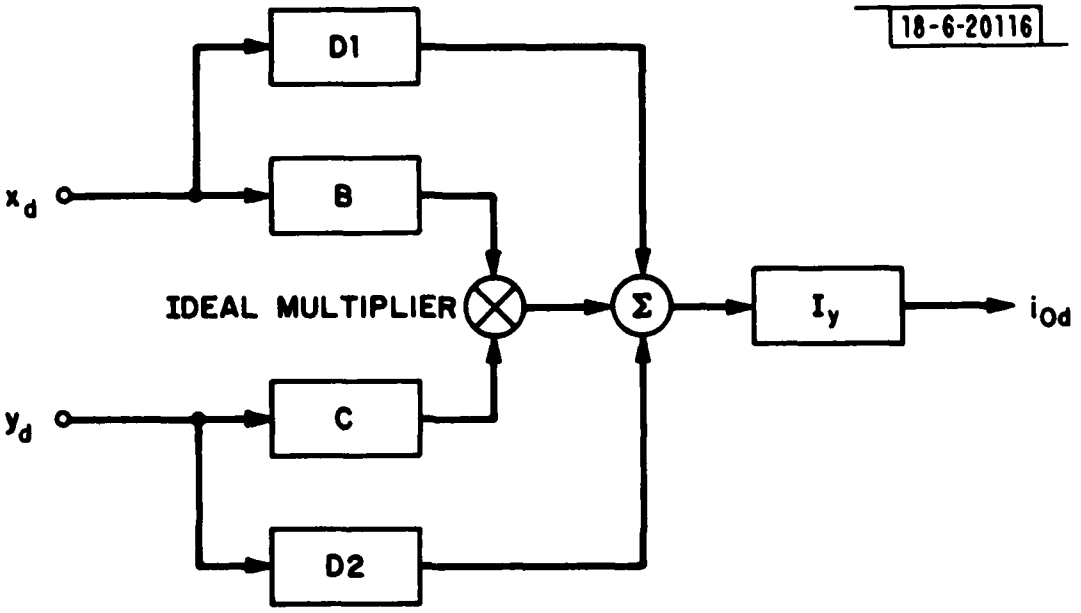

Fig. 5. Model for non-ideal transconductance cell at DC.

$b_2 x_d^2$ ($c_2 y_d^2$) – quadratic non-linearity in the x(y) signal path

$b_3 x_d^3$ ($c_3 y_d^3$) – cubic non-linearity in the x(y) signal path

$d_0 I_y$ – equivalent output offset

$d_1 x_d I_y$ ($d_2 y_d I_y$) – x(y) feedthrough

$d_3 x_d^2 I_y$ ($d_4 y_d^2 I_y$) – x(y) quadratic feedthrough

$d_5 x_d^3 I_y$ ($d_6 y_d^3 I_y$) – x(y) cubic feedthrough

$d_7 x_d^4 I_y$ ($d_8 y_d^4 I_y$) – x(y) quartic feedthrough

$b_1 c_1 x_d y_d I_y$ – the desired response; if $b_1 c_1 \neq 1$, this constitutes a scale factor error.

Gilbert has analyzed and verified the important sources of error for static operation when the circuit is operated in a purely differential manner. The causes and effects can be summarized as follows (for a more complete and quantitative discussion, see Ref. 2).

1. Emitter Area (v_{BE}) Mismatch

   Errors of this type within the quad $Q_1 Q_2 Q_5 Q_6$ and/or the quad $Q_3 Q_4 Q_5 Q_6$ will introduce:

   A. An equivalent offset in the x signal path

   B. An equivalent output offset

   C. A quadratic non-linearity in the x signal path

   D. An x quadratic feedthrough term

   E. No y offset, non-linearity, or feedthrough

2. Thermal Gradients

   A. Gradients across individual pairs Q_1Q_2, Q_3Q_4, Q_5Q_6 cause equivalent input offset errors.

   B. Temperature differences between the quad $Q_1Q_2Q_3Q_4$ and the pair Q_5Q_6 introduce a cubic non-linearity in the x signal path.

   C. Thermal offsets do not cause y non-linearity or feedthrough.

3. Finite Large-Signal Current Gain (β)

   A. If β is constant, but finite, and well-matched between transistors over the operating range it will introduce only a scale factor error.

4. Resistive Mismatch

   Equivalent resistances in the emitters of the transistors, as in Fig. 6 (these are generally reflected from the base circuits of the transistors), can cause errors of the following type if $R_1 = R_2 = R_3 = R_4$ and $R_5 = R_6$:

   A. There is a cubic non-linearity in the x signal path, as well as a scale factor error.

   B. There is no y offset, non-linearity, or feedthrough.

   C. No distortion arises when $R_1I_y = R_2I_y = \ldots = R_5I_x = R_6I_x$.

   Additionally, if $R_1 \neq R_2 \neq R_3 \neq R_4$:

   D. There will be non-linear x feedthrough having an s-shaped characteristic; i.e., primarily first and third order components.

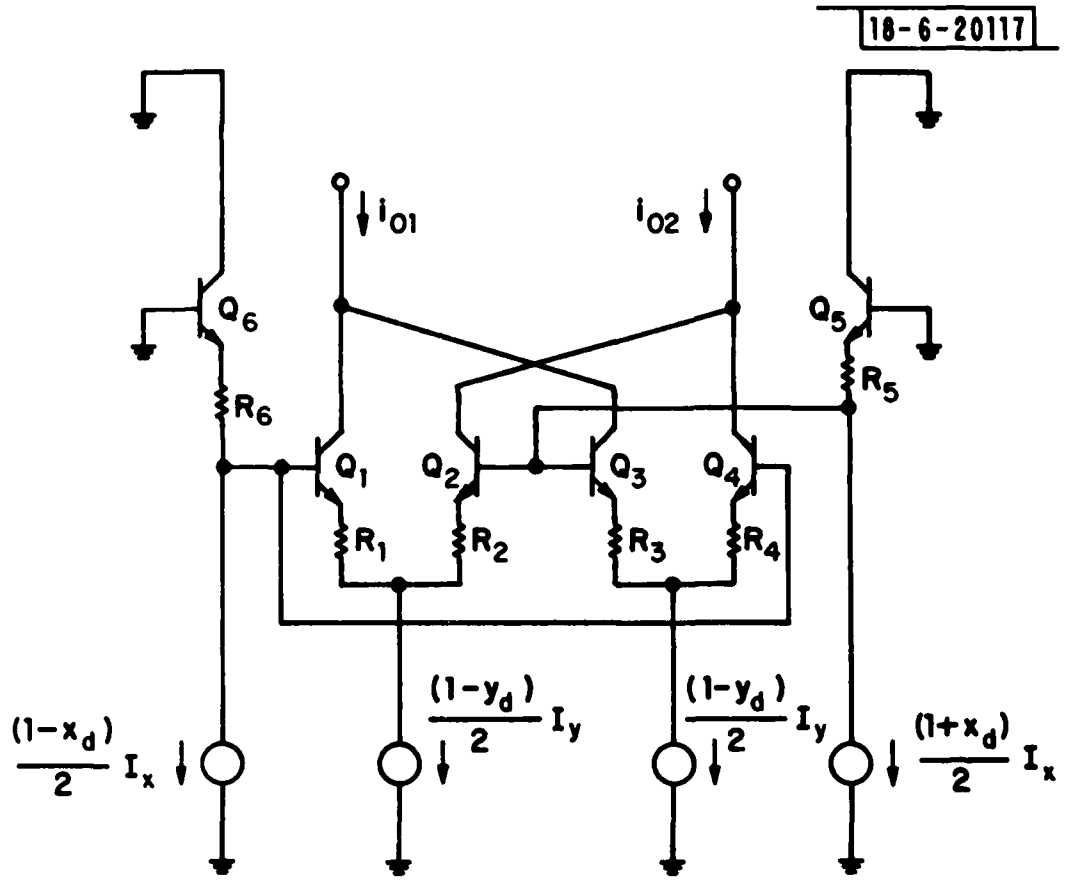

Fig. 6. Resistive errors in transconductance cell.

If these error sources are small, then they may be considered relatively independent and their effects assumed additive. The resulting model is described by

$$i_{od} \tilde{=} [(b_3 x_d^3 + b_2 x_d^2 + b_1 x_d + b_0)(c_1 y_d + c_0) + (d_0 + d_1 x_d + d_3 x_d^2 + d_5 x_d^3)] I_y \quad (17)$$

It was decided early, in light of this analysis, to make the y input port the RF, or signal, input and the x input port the DC, or control, input. This was based on the following considerations:

1. The y input path is inherently the more linear of the two, and linearity in the RF path is a more critical requirement than in the control path. With this choice, static non-linearity in the RF path is a function of the input voltage-to-current conversion almost exclusively, not of errors in the transconductance cell.

2. Residual non-linearity in the control path is tolerable because the weights are driven closed-loop in the nulling system. Furthermore, any feedthrough from the control input is outside the signal bandwidth.

3. Static errors in the transconductance cell do not cause feedthrough from the y input. This is important in trying to minimize RF feedthrough.

The decision was also made not to correct any DC offset errors. These are not critical because the RF path is AC coupled and the control path is in a closed-loop system.

IV. COMMON-MODE ERRORS

It has been shown that the presence of frequency-dependent feedthrough errors in weight circuits can substantially limit the performance of a nulling system (Ref. [3]). A requirement of low feedthrough translates into a need for a multiplier that can achieve a good depth-of-null across the band of interest.

Inspection of Fig. 1 shows that the operation of the multiplier depends upon the generation of two currents, i_{y1} and i_{y2}, that are incrementally 180° apart. Achieving a good depth-of-null depends upon accurate vectoral cancellation of these currents. In fact, the two problems associated with attaining a good null in a transconductance multiplier are the elimination of true feedthrough paths (i.e., stray coupling) and the elimination of tracking errors in the differential path. The existence of the latter problem makes transconductance multipliers qualitatively different from weight circuits that use true attenuation, in which no vectorial cancellation is involved.

The presence of tracking errors can always be expressed by the addition of a common mode signal. To illustrate, let

$$i_{y1} = \frac{(1+y_d+y_c)}{2} I_y$$

$$i_{y2} = \frac{(1-y_d+y_c)}{2} I_y \tag{18}$$

where

$$y_d = \frac{i_{y1}-i_{y2}}{I_y}$$

$$y_c = \frac{i_{y1}+i_{y2}-I_y}{I_y} \tag{19}$$

and y_c represents a common mode signal at the input to the transconductance cell. Then the differential output is

$$i_{od} = x_d y_d I_y \tag{20}$$

and the common mode output can be defined as and determined to be

$$i_{oc} = i_{o1} + i_{o2} - I_y$$

$$= y_c I_y \quad . \tag{21}$$

If the output differencing circuit (to produce i_{o1}-i_{o2}) does not have sufficient common mode rejection then, for AC signals, a deep null is not possible.

For example, let

$$i_{y1} = \frac{1}{2}\{1 + A\cos\omega t\} I_y$$

$$i_{y2} = \frac{1}{2}\{1 - A\cos(\omega t+\phi)\} I_y \tag{22}$$

then

$$i_{od} = x_d I_y A \cos\frac{\phi}{2} \cos(\omega t + \frac{\phi}{2})$$

$$i_{oc} = I_y A \sin\frac{\phi}{2} \sin(\omega t + \frac{\phi}{2}) \tag{23}$$

If the common-mode output signal is not suppressed, then the output at null (x_d=0) will consist of a signal in quadrature with the full-scale output. Experimentally, this may appear to be the result of a capacitive feedthrough path. This effect is shown vectorally in Fig. 7. If a single-ended output is used (i.e., either i_{o1} or i_{o2}) then the maximum depth of null is, for small ϕ,

$$\left|\frac{i_{oc}}{(i_{od})_{max}}\right| = \left|\frac{y_c}{y_d}\right| = \left|\frac{\sin\frac{\phi}{2}}{\cos\frac{\phi}{2}}\right| \simeq \left|\frac{\phi}{2}\right| \quad . \tag{24}$$

For example, if $\phi = 1° = 17.45 \times 10^{-3}$ rad, then the maximum depth of null is given by

$$20 \log_{10}\left(\frac{17.45 \times 10^{-3}}{2}\right) = -41.2 \text{ dB} \quad . \tag{25}$$

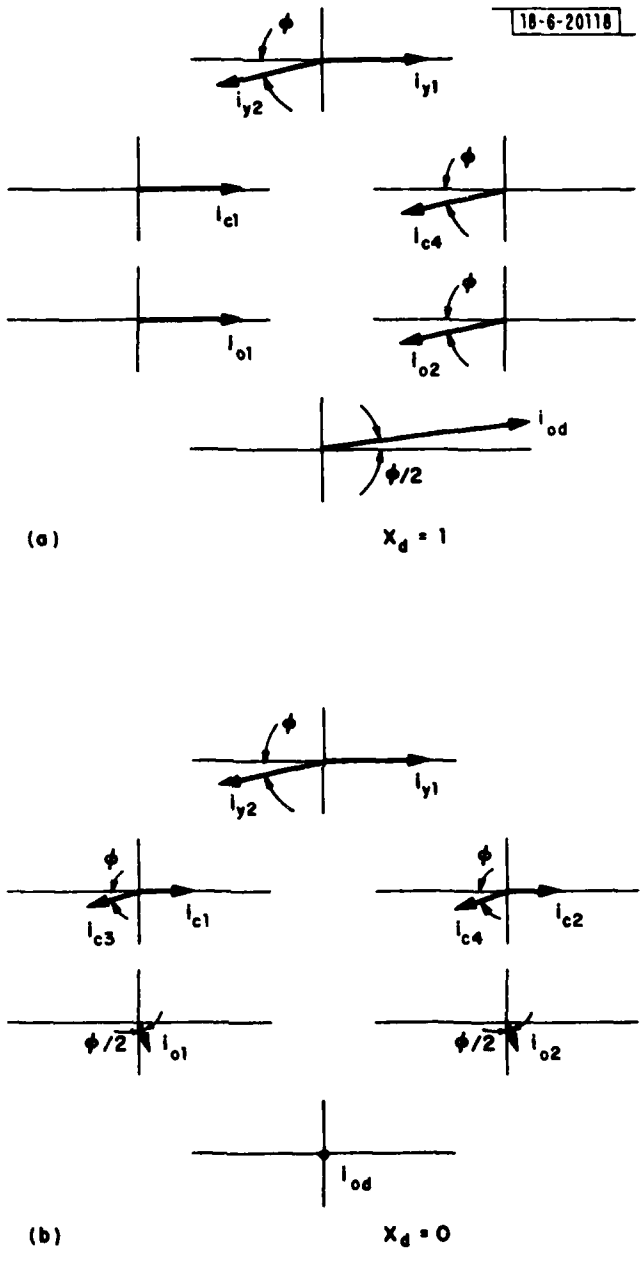

Fig. 7. Vectorial representation of ideal transconductance cell incremental currents for two values of x_d. (Common mode input errors assumed.)

This effect was observed in early prototypes. When the RF input was applied in a single-ended fashion to a differential stage to produce i_{y1} and i_{y2}, and the output was taken from only one side of the differential output, null depths were limited to approximately 13 dB. Interestingly, this effect is (ideally) absent from the x input. When the RF signal was applied in a similar fashion to this input in prototypes, null depths of 25 to 30 dB were obtainable.

The reduction of the effects of this source of error to acceptable levels requires true differential drive at the RF input and true differential detection at the output. This was achieved in the final circuit by using center tapped transformers at both input and output, as can be seen in the schematic shown in Fig. 8. In this way, common mode generation and response at the input and output, respectively, were suppressed by 35 to 40 dB.

V. SECOND-ORDER ERRORS

Multipliers constructed along the guidelines discussed thus far can readily achieve broadband (50 MHz, about our center frequency of interest) nulls of 45 to 50 dB and better, given proper attention to layout, transistor selection, operating current, etc. For some units, nulls of greater than 65 dB over a 10 MHz band (same center frequency) have been documented. At this level, isolating and verifying residual sources of error becomes very difficult at 120 MHz. This section discusses another error mechanism that is qualitatively consistent with observed behavior, but that has not, to date, been confirmed experimentally. It illustrates the type of interaction that may be expected between common-mode signals and transconductance cell non-ideality.

In prototype multipliers, the following behavior was observed:

1. The addition of an input transformer, to provide balanced drive, generally increased the achievable depth-of-null by an amount consistent with the reduction of the common-mode component of the current drive to the transconductance cell. However, the subsequent addition of a balanced output transformer resulted in far less improvement in the depth-of-null.

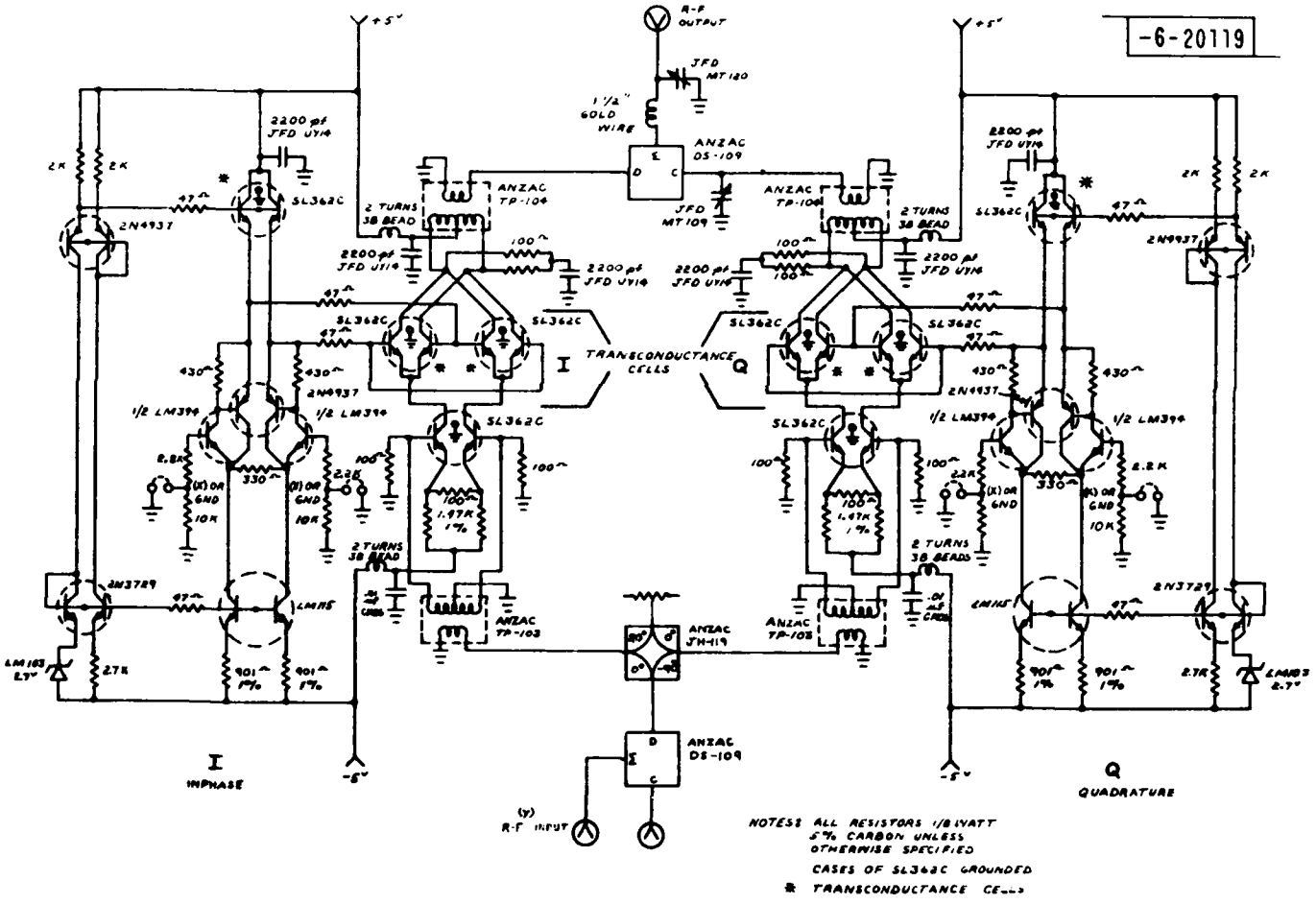

Fig. 8. Transconductance multiplier weight circuit schematic.

2. Increasing quiescent current I_y always deteriorated the achievable depth-of-null. This effect was more pronounced in some units than in others.

The effect of resistive mismatch, shown in Fig. 2, in the presence of common-mode signals can be derived in a manner similar to Gilbert's (Ref. [2], p. 369). It can be shown that if

$$i_{y1} = \frac{(1+y_d+y_c)}{2} I_y$$

$$i_{y2} = \frac{(1-y_d+y_c)}{2} I_y \tag{26}$$

Then, to a first approximation

$$i_{od} = x_d y_d I_y + \left(\frac{1-x_d^2}{4}\right) \left\{ -2y_d(1+y_c)\left[x_d\xi_{yc}+\xi_{ydb}\right] - \left[(1+y_c)^2 + y_d^2\right]\left[x_d\xi_{yda}+\xi_{ydc}\right] + 2x_d y_d \xi_{xc} + 2y_d \xi_{xd} \right\} I_y \tag{27}$$

where

$$\xi_{yc} = \left[\frac{R_1+R_2+R_3+R_4}{4}\right]\frac{qI_y}{kT}$$

$$\xi_{yda} = \left[\frac{R_1+R_2-R_3-R_4}{4}\right]\frac{qI_y}{kT}$$

$$\xi_{ydb} = \left[\frac{R_1-R_2+R_3-R_4}{4}\right]\frac{qI_y}{kT}$$

$$\xi_{ydc} = \left[\frac{R_1-R_2-R_3+R_4}{4}\right]\frac{qI_y}{kT}$$

$$\xi_{xc} = \left[\frac{R_5+R_6}{2}\right]\frac{qI_y}{kT}$$

$$\xi_{xd} = \left[\frac{R_5-R_6}{2}\right]\frac{qI_y}{kT} \tag{28}$$

Note that, for well matched resistances, ξ_{yc} and ξ_{xc} will be the dominant terms.

The expression for the output can be decomposed as

$$\begin{aligned} i_{od} = {} & y_d \left\{ x_d^3 \left[\tfrac{1}{2}\xi_{yc} - \tfrac{1}{2}\xi_{xc} \right] + x_d^2 \left[\tfrac{1}{2}\xi_{ydb} - \tfrac{1}{2}\xi_{xd} \right] \right. \\ & \left. + x_d \left[1 - \tfrac{1}{2}\xi_{yc} + \tfrac{1}{2}\xi_{xc} \right] + \left[-\tfrac{1}{2}\xi_{ydb} + \tfrac{1}{2}\xi_{xd} \right] \right\} I_y \\ & + y_c \left\{ x_d^3 \left[\tfrac{1}{2}\xi_{yda} \right] + x_d^2 \left[\tfrac{1}{2}\xi_{ydc} \right] \right. \\ & \left. + x_d \left[-\tfrac{1}{2}\xi_{yda} \right] + \left[-\tfrac{1}{2}\xi_{ydc} \right] \right\} I_y \\ & + \left\{ x_d^3 \left[\tfrac{1}{4}\xi_{yda} \right] + x_d^2 \left[\tfrac{1}{4}\xi_{ydc} \right] \right. \\ & \left. + x_d \left[-\tfrac{1}{4}\xi_{yda} \right] + \left[-\tfrac{1}{4}\xi_{ydc} \right] \right\} I_y \\ & + (\text{higher order } y \text{ terms and products}) \quad . \end{aligned} \tag{29}$$

This expression is consistent with that derived by Gilbert, but is more complete. In particular, note the equivalent cubic non-linearity introduced in the x signal path, as well as the non-linear x feedthrough term.

When x_d is set to minimize the output (i.e., $x_d \tilde{=} 0$), then (ignoring offsets and higher order terms, which will be outside the bandwidth of interest),

$$i_{od} \tilde{=} y_c I_y \left[-\tfrac{1}{2}\xi_{ydc} \right] \quad . \tag{30}$$

This sets a limit on the depth of null achievable in the presence of common-mode signals and resistive mismatch. This is

$$\left| \frac{(i_{od})_{min}}{(i_{od})_{max}} \right| \simeq \left| \left[\frac{y_c}{y_d} \quad \frac{1}{2} \xi_{ydc} \right] \right| \quad . \tag{31}$$

For instance, if

$$\left[\frac{R_1 - R_2 - R_3 + R_4}{4} \right] I_y = 6 \text{ mV} \tag{32}$$

then

$$\xi_{ydc} \simeq \frac{1}{4} \tag{33}$$

and the improvement in null depth over that achievable without a balanced output (as given by Eq. 24) is limited to

$$20 \log_{10} \left(\frac{1}{2} \xi_{ydc} \right) \simeq -18 \text{ dB} \quad . \tag{34}$$

Furthermore, as the quiescent current I_y is increased the achievable depth of null will decrease proportionately, through the dependence of ξ_{ydc} on I_y as given by Eq. 28.

For low frequency applications, where I_y is usually limited to a few hundred microamperes and large geometry transistors are used, this error source may be negligible. For RF circuits, where I_y may be several milliamperes and small geometry devices must be used, it may be significant.

In general, the emitter resistors of Fig. 6 can probably be more accurately modeled as complex impedances, reflecting, in part, the complex impedances seen by the bases of the transistors. The effects of these components could be similarly decomposed into common-mode and differential parts to determine the resulting system response.

It can be shown that mismatches in temperature, area, and β between transistors in the transconductance cell can also result in common mode input current being transformed to differential output current. It can be shown that these second-order effects are small and relatively independent of operating current, and analytical expressions are not presented here.

VI. IN-PHASE, QUADRATURE, AND FEEDTHROUGH SIGNALS

A complete weight circuit includes two multipliers whose inputs are driven in quadrature from a 90° power splitter and whose outputs are summed with a 0° power combiner as shown previously in Fig. 2. The two independent control inputs thus allow adjustment of the weight's transfer function over all possible phase angles and magnitudes (up to some maximum).

For small common-mode errors (equivalently, small internal tracking errors) the output of a non-ideal multiplier at null will be a signal very nearly in quadrature with the full-scale output as in the example presented earlier. In a complete weight circuit, any such effect in one multiplier can be modeled as an equivalent offset in the control input of the other multiplier, so that the null depth achievable in a complete weight circuit should be much greater than that achievable by either multiplier alone. A similar argument can be made regarding any input-to-output paths that are the result of stray coupling.

This cancellation effect is limited if these feedthrough* paths do not have the same frequency-dependence as the controllable paths through the multipliers. If this is the case, deep nulls are achievable only over limited bandwidths.

---

*It will be useful from this point to use the term "feedthrough" to refer to any input-to-output path over which the control voltage has no influence, whether this path is a result of internal tracking errors and device mismatch or true stray coupling. Functionally, this difference is academic.

The weights constructed using these multipliers typically reached null depths of 65 dB over 10 MHz. It did not matter if the individual multipliers could reach 65 dB or were limited to 50 dB.

VII. DESIGN AND CONSTRUCTION

A schematic of one complete weight circuit is shown in Fig. 8* and a photograph in Fig. 9. The transconductance cells and the voltage-to-differential current stages for the RF and control inputs are readily identifiable. The 47Ω resistors in the base leads of the transistors in the transconductance cells were used to damp a troublesome resonance. It was also found to be advantageous to ground the cans of the RF transistors (Plessey SL-362C monolithic duals) to a common point. Quiescent current was set such that $I_x = I_y = 6$ mA.

Special attention was given to developing a layout with symmetrical paths for the differential RF signal. This was generally achieved except in the base circuits of the transconductance cell, where two-dimensional layout constraints prevailed.

The LC matching network at the output was designed to improve the output impedance over the bandwidth of interest. Additionally, the capacitor was used to match unit-to-unit group delays. The other variable capacitor was used to trim the differential delay between the I and Q sides of the weight. This procedure will be described later.

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*Note that each circuit contains a 0° power splitter at the input that is not part of the weight proper but was placed in the same box out of system considerations. All the measurements relating to weight circuit performance include the effects of this splitter.

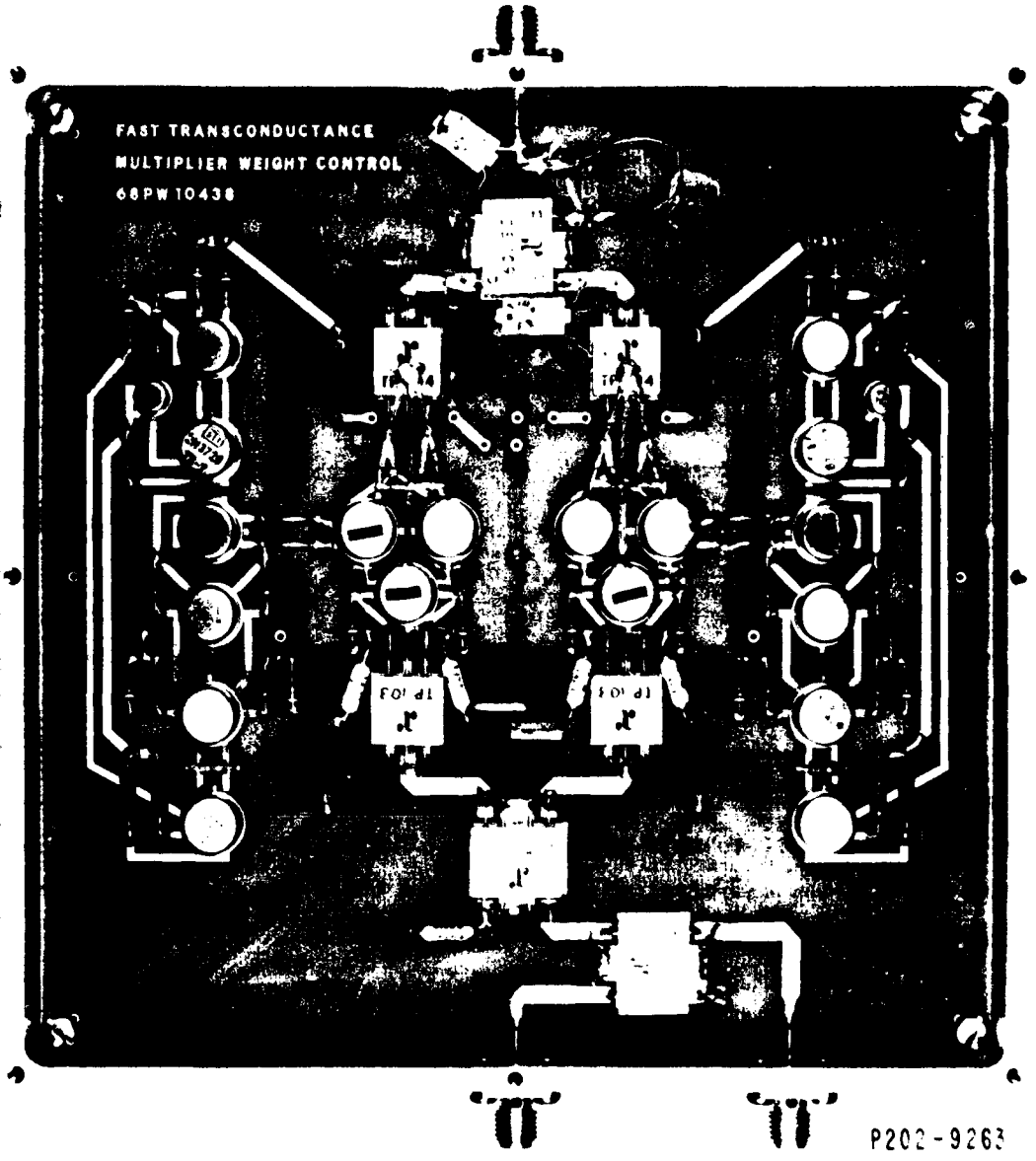

Fig. 9. Photograph of weight circuit.

VIII. MEASURED PERFORMANCE

Figures 10 thru 16 illustrate the measured performance of the weights. Figure 10 shows the inherent linearity of a single multiplier over most of the operating range of the control voltage. (The measurements for this graph were made on a prototype multiplier, where maximum v_x was designed to be slightly more than 1.5 volts. For the multipliers in the actual weights, this value was re-scaled to be 1.0V. Because the departure from linearity is almost exclusively a function of the characteristics of the transconductance cell, re-scaling has little effect on linearity.) The measurements were made at a single frequency near 120 MHz. From each point, a feedthrough term (i.e., the residual output of the multiplier when the control voltage was set for maximum attenuation) was subtracted off, so the curve is referenced to only that component of the input signal over which gain control can be exerted. Of particular interest is the odd symmetry of the dominant non-linearities, especially the obvious third-order term. This indicates again that the primary error source in the transconductance cell is resistive. It is of interest to note that commercially available transconductance multipliers only allow the x and y inputs to operate over a fraction (typically 0.5 to 0.75) of their possible range to avoid the larger departures from linearity visible in Fig. 10. For this application, noise considerations precluded this approach.

Figure 11 shows the amplitude response of one weight circuit with V_I and V_Q adjusted for minimum response at center frequency. Similar measurements on the other seven circuits yield very similar results.

Figures 12 thru 16 and Table 1 show the results of several conventional two-port measurements on one weight circuit with V_I = 1.0V and V_Q = 0.0V. They are self-explanatory and, again, representative of all the weights.

TABLE 1

TRANSCONDUCTANCE MULTIPLIER WEIGHT CHARACTERIZATION

VI = 1.0V VQ = 0.0V

Freq.-MHz	Gain-dB Forward	Phase Forward	RTN Loss Forward	VSWR Forward	RTN Loss Reverse	VSWR Reverse
111.400	-12.86	6.78	37.08	1.03	19.48	1.24
112.400	-12.85	4.78	37.20	1.03	19.69	1.23
113.400	-12.85	2.76	37.22	1.03	19.92	1.22
114.400	-12.84	.74	37.13	1.03	20.14	1.22
115.400	-12.84	- 1.26	37.13	1.03	20.38	1.21
116.400	-12.83	- 3.30	37.10	1.03	20.61	1.21
117.400	-12.83	- 5.23	37.06	1.03	20.84	1.20
118.400	-12.82	- 7.26	36.91	1.03	21.09	1.19
119.400	-12.82	- 9.20	36.88	1.03	21.33	1.19
120.400	-12.79	-11.29	36.78	1.03	21.64	1.18
121.400	-12.79	-13.41	36.51	1.03	21.86	1.18
122.400	-12.78	-15.40	36.56	1.03	22.03	1.17
123.400	-12.76	-17.44	36.56	1.03	22.25	1.17
124.400	-12.77	-19.39	36.44	1.03	22.44	1.16
125.400	-12.78	-21.45	36.41	1.03	22.58	1.16
126.400	-12.79	-23.43	36.34	1.03	22.70	1.16
127.400	-12.79	-25.49	36.22	1.03	22.74	1.16
128.400	-12.80	-27.43	35.97	1.03	22.85	1.16
129.400	-12.80	-29.47	35.90	1.03	22.83	1.16
130.400	-12.80	-31.47	35.83	1.03	22.76	1.16
131.400	-12.80	-33.70	35.65	1.03	22.66	1.16

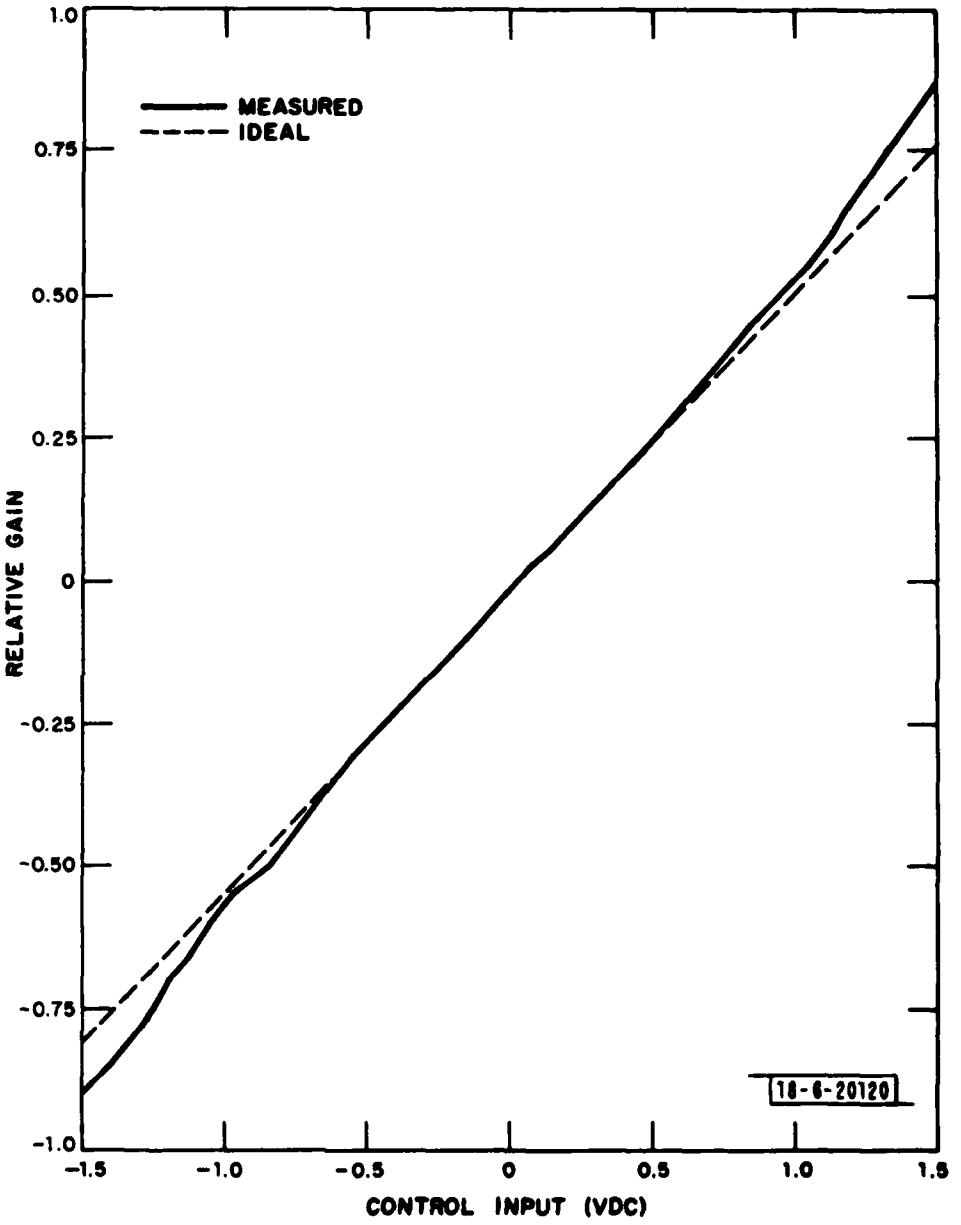

Fig. 10. Multiplier gain vs control input.

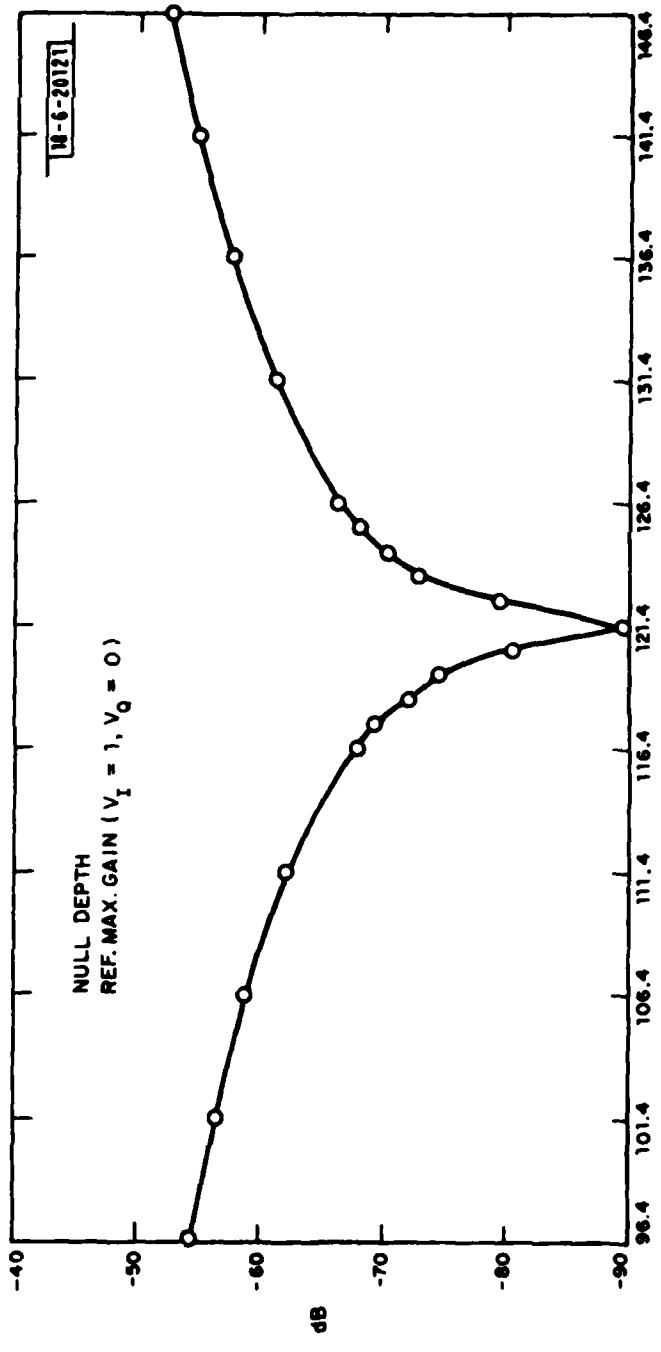

Fig. 11. Weight circuit null depth.

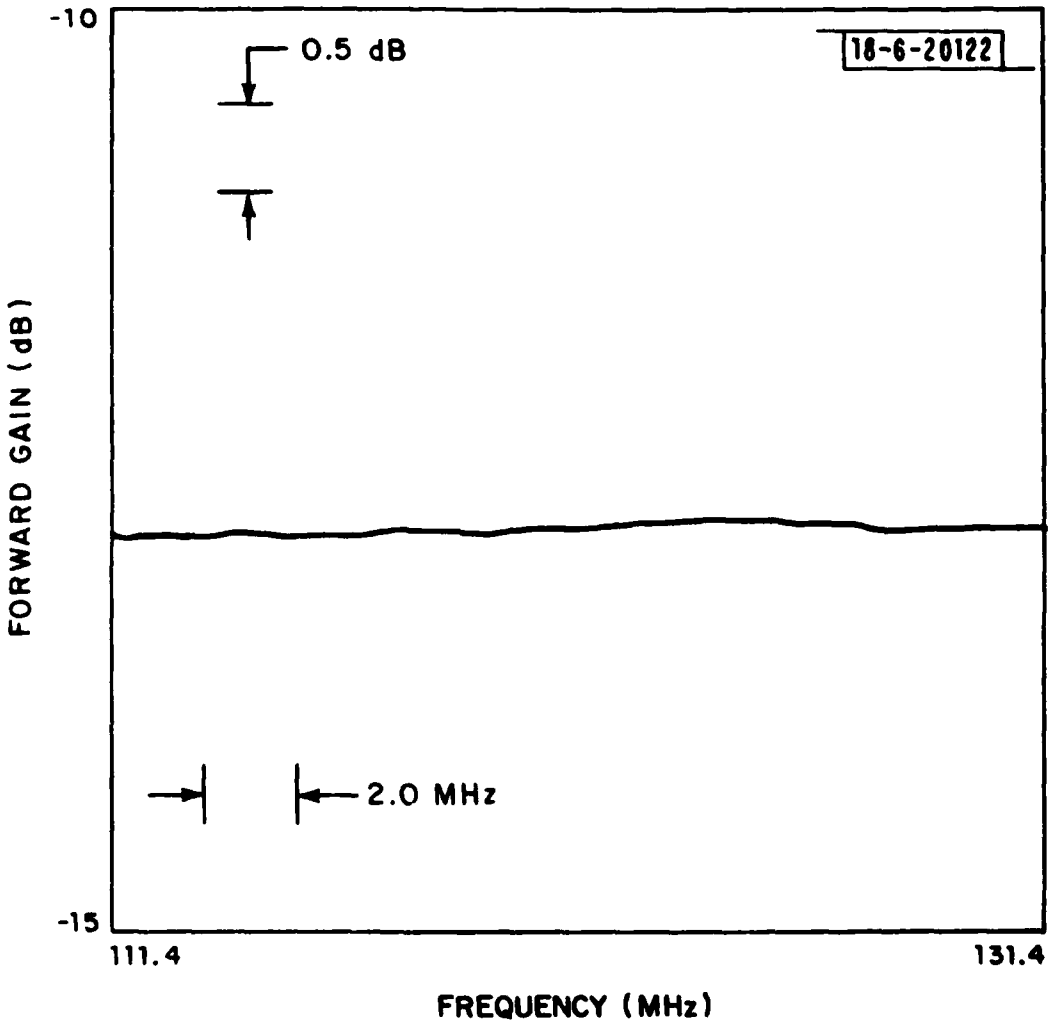

Fig. 12. Transconductance multiplier weight characterization: forward gain.

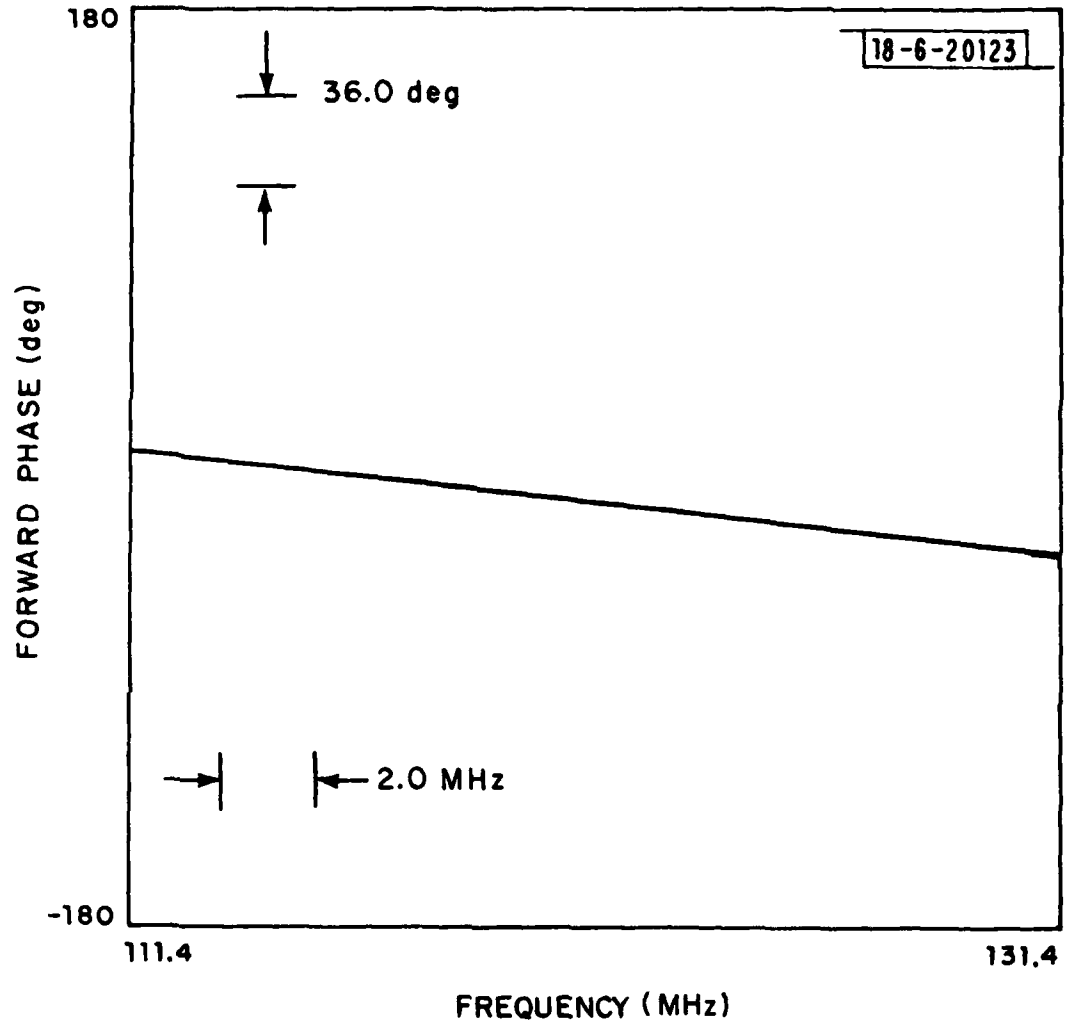

Fig. 13. Transconductance multiplier weight characterization: forward phase response.

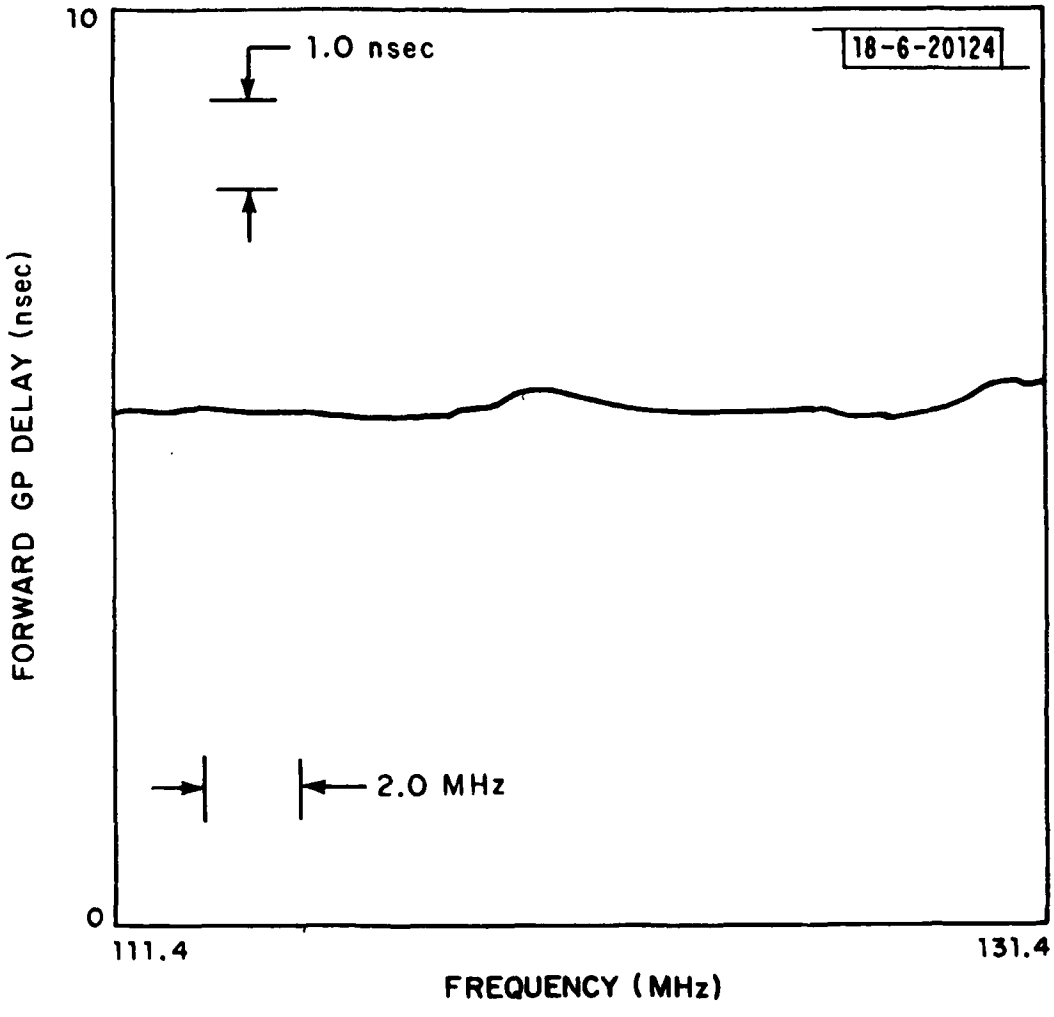

Fig. 14. Transconductance multiplier weight characterization: forward group delay.

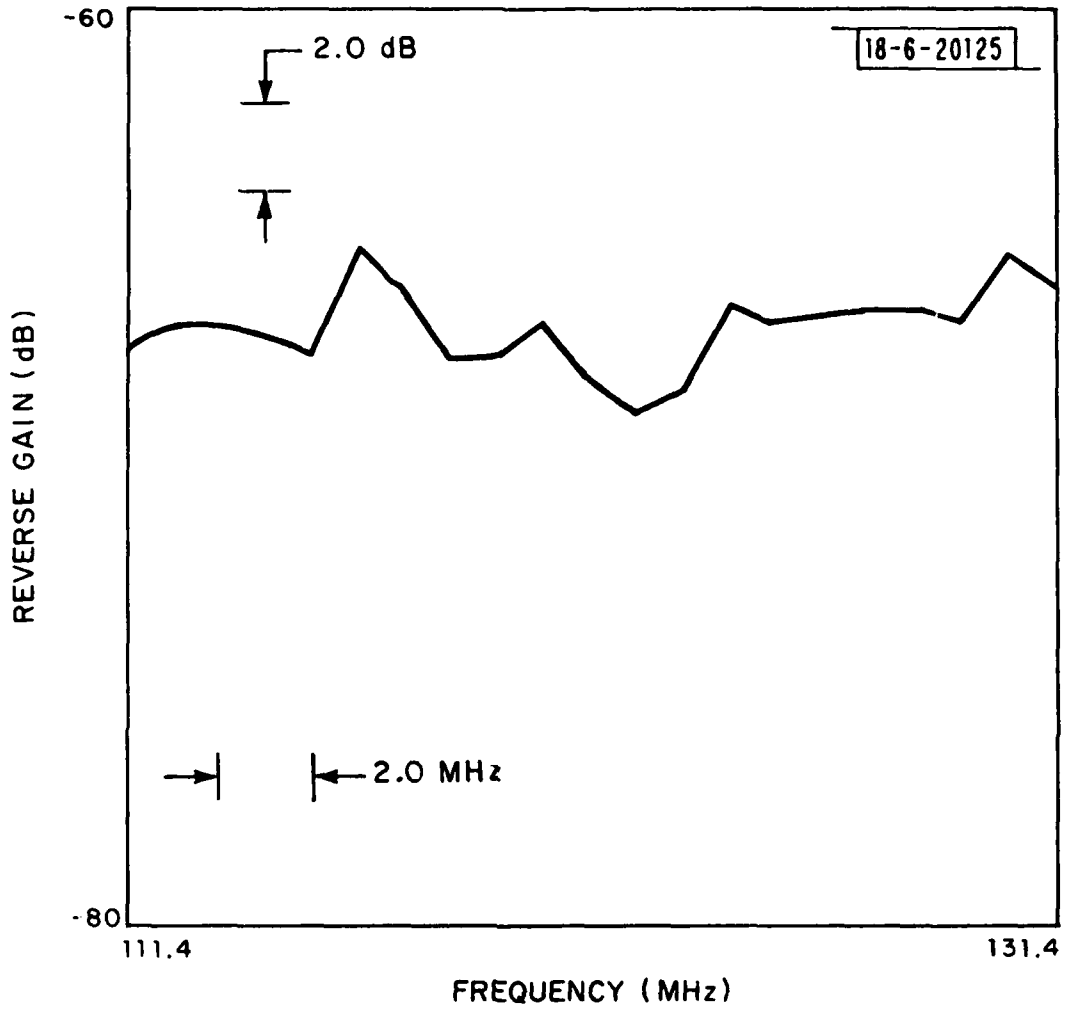

Fig. 15. Transconductance multiplier weight characterization: reverse gain.

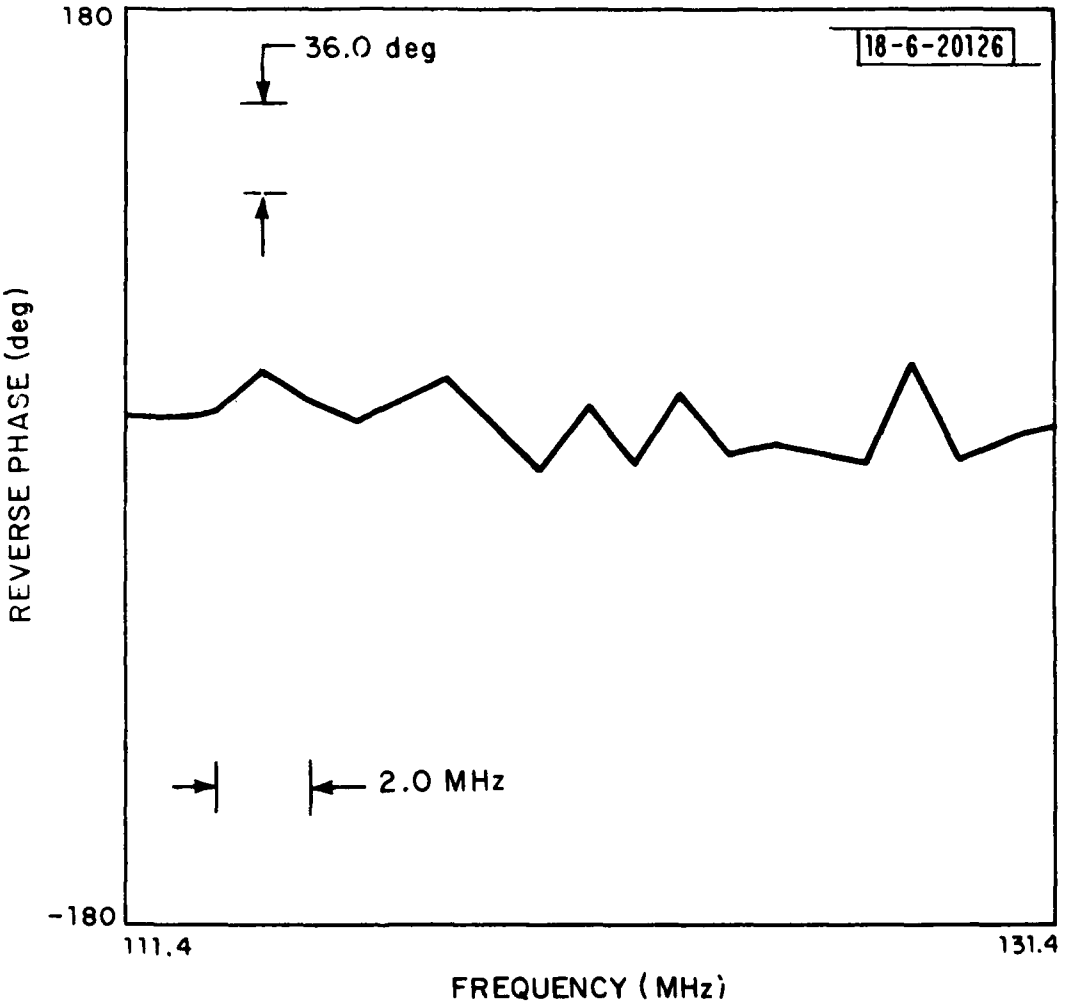

Fig. 16. Transconductance multiplier weight characterization: reverse phase response.

Results of other measurements, taken with a 1,0 or 0,1 control voltage setting are as follows:

Gain:	− 13 dB
1 dB Compression:	2.5 dBm
Noise Figure:	22 to 23 dB

Power consumption of each weight is 280 mW.

IX. TRACKING ADJUSTMENTS

The presence of tracking errors in the weights (i.e., non-uniform amplitude and phase slopes from unit to unit) can result in a significant depth-of-null degradation in a nulling system [Ref. (4)]. Because of the inherently wide bandwidth of the weights, tracking errors were primarily the result of group delay mismatch.

The group delays were equalized between units by adjusting the capacitor in the output impedance matching network. These adjustments were small enough to leave the output VSWR essentially unaffected. Additionally, any differential delay between the in-phase and quadrature paths in each weight was adjusted with a small shunt capacitor at the output of the appropriate multiplier.

The setup for performing the tracking adjustments is shown in Fig. 17. One weight was chosen as a reference, and its differential delay was trimmed as accurately as possible. Each remaining weight was subsequently trimmed to match the reference by adjusting V_I, V_Q, and the trim points to obtain the best possible null across the band of interest. (The orthogonality of the in-phase and quadrature paths made this procedure somewhat simpler than it may appear.) The consistency of the trims was checked for several settings of V_I and V_Q.

The 0° power splitters in Fig. 17 were selected for high accuracy across the band, but to establish confidence in their matching a final check was made by reversing the position of the reference weight and one of the adjusted weights. It was found that the attainable depth-of-null had not appreciably deteriorated.

After trimming, the weights were measured for tracking errors and eigenvalue plots were generated. Nulling simulations, using an automated test system, were performed on sets of four weights. (See Ref. [5] for a description of these procedures.)

X. CONCLUSION

The virtual elimination of feedthrough in the weights enabled the nulling system to achieve its objectives for depth-of-null performance (Ref. [6]). This performance is consistent with the tracking measurements made on the individual weights, and indicates that improvement of channel tracking is a potentially fruitful area for further research.

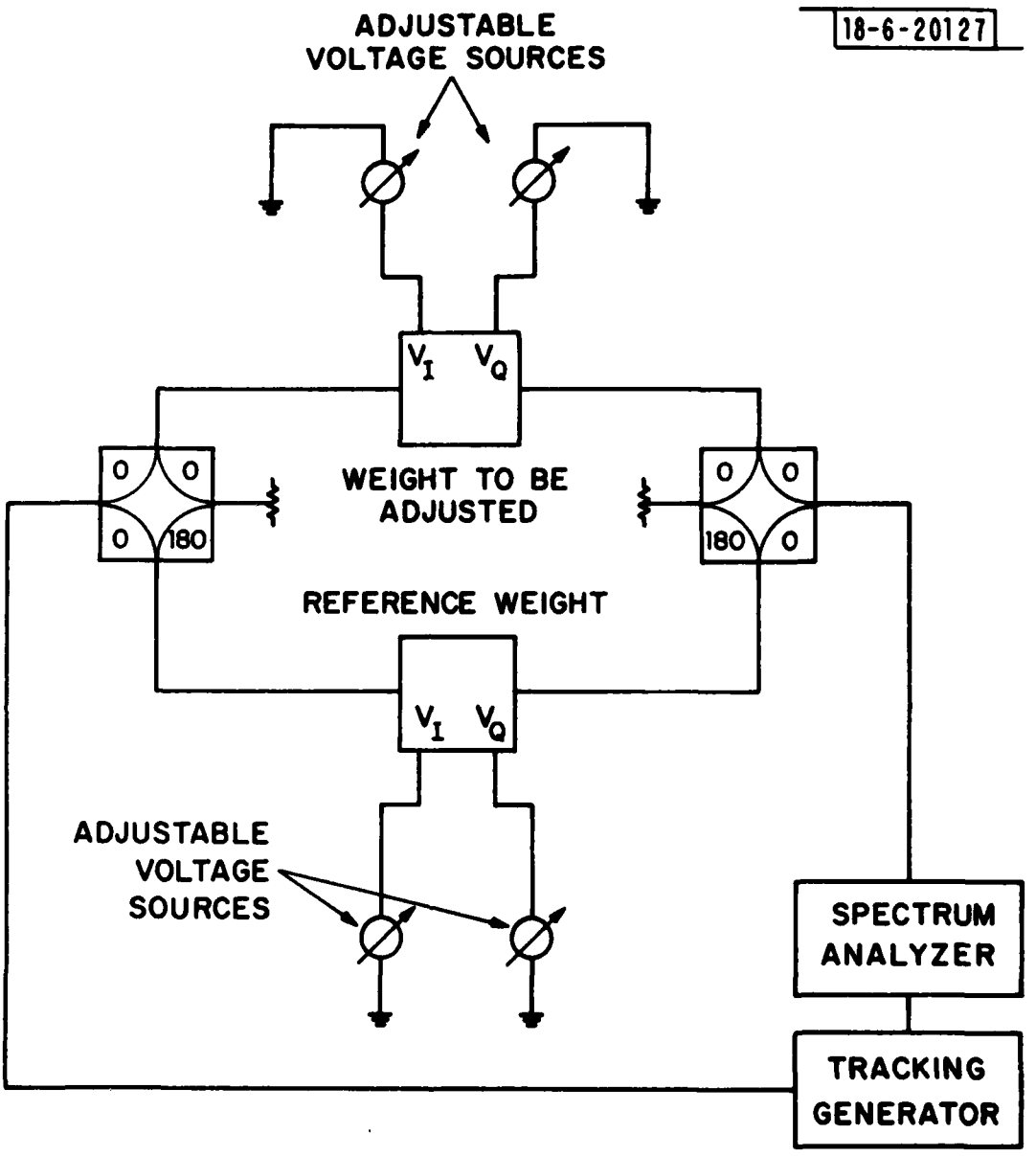

Fig. 17. Setup for tracking adjustments.

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The design, construction, and measurement of weight circuits utilizing four-quadrant transconductance multiplication is described. The weights operate over a 10 MHz band centered at 121.4 MHz.

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